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Calculation and Development of Analog-Digital Converters with Signal Measurement Range

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Abstract – An analog-to-digital converter with compression of the measurement range must have a functional quantization characteristic that depends on the a priori distribution law of the measured signal. For the logarithmically uniform distribution law of the signal, which is most common in information and measuring technology, the quantization characteristic (for converters with a linear transformation characteristic) must have a constant relative quantum value. In this regard, the development of an analog-to-digital converter with a functional conversion characteristic is urgent.

Keywords – Spectrometry, Devices For Preliminary Processing Of Information, Analog-Digital Converters.

I. INTRODUCTION

In information and measuring technology, transducer circuits with a quasi-optimal quantization scale with automatic switching of measurement limits, the values of which, as a rule, correspond to a geometric series and, therefore, obey the optimal quantization law, have become widespread [1]. Within the measurement limits, a linear quantization scale is used. A large number of works have been devoted to the development of measuring transducers [2], however, most of the developed schemes use the principle of switching the limits after the completion of the next transformation, which leads to skipping measurements with frequent switching of limits [3].

To a certain extent, the converter circuits developed by the author with automatic selection of the measurement limit directly in the process of converting the measuring signal are free from this drawback [4].

In fact, such converters allow you to get the code at the output input signal in normal form (floating point), consisting of mantissa code and characteristic code.

Converters of this kind, developed with the participation of the author [5], can use the well-known principles of analog - digital conversion - bitwise balancing, frequency conversion, integration [6].

II. RESULT AND DISCUSSION

The principle of operation of the converter of the integrating type is integrating the signal U_x with the time constant t_u and comparing the integrated signal $U_u = U_x \frac{t}{t_u}$ with the voltage $\frac{U_0}{a}$, where a - is the base of the numeral system of the characteristic code, U_0 is the voltage corresponding to the upper limit of the dynamic range of U_x. At the same time, the time intervals $t1$, $a\,(t1)$,..., a^{n_h} $(t1)$ are formed.

The U_x signal is integrated to the nearest time moment $t_{ui} = a^i t1$, next after the moment t_c comparing the voltages U_u and $U_{0/a}$. At the end of the integration, the voltage U_u is equal to

$$U_u = U_x \frac{t_{ui}}{t_u} = U_x a^i \frac{t1}{t_u}.$$

The number of the integration interval, obviously, determines the N_H characteristic code, the mantissa code is determined after converting the voltage U_u by any of the known analog-to-digital conversion methods.

Conversion duration (actually - integration time)

the speed of the analog-to-digital converter when converting a signal in the upper part of its range is its advantage.

A similar analog-to-digital converter circuit [7] can be built on the basis of pulse-frequency conversion (Fig.1).

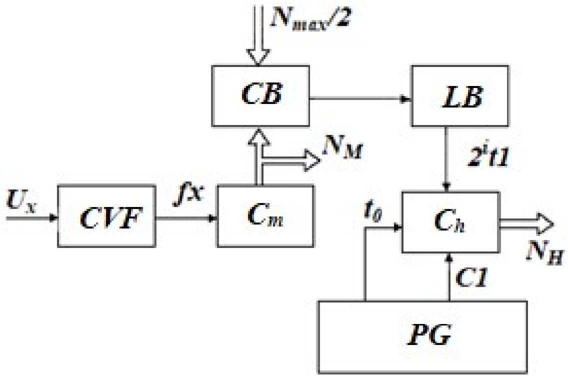

Fig. 1 - Scheme of an analog-to-digital converter with frequency conversion of the signal and with automatic determination of the characteristic code during the conversion of the signal

Here, the role of the integrator is played by the counter of the pulses arriving at its input from the output of the "voltage - frequency" converter (VFC).

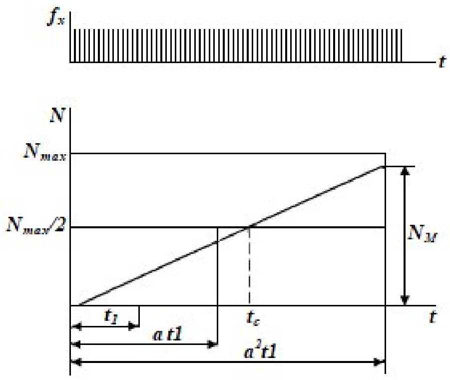

Fig. 2 - Diagram of the operation of an integrating converter with a frequency signal conversion and automatic determination of the measuring range

The *CC*-code comparison block plays the role of a comparator. Its inputs receive the code from the outputs of the counter C_v and the code $N_{max}/2$, half the code of its maximum capacity. The characteristic code N_h is taken from the outputs of the counter C_v, the code of the mantissa - from the outputs of the counter C_m. The pulse generator generates counting pulses *c1*, and also forms an interval

time t_0.

The U_f pulses generated by the voltage-frequency converter (Fig. 2), the frequency of which is proportional to the value of the input signal U_x, are fed to the mantissa counter C_m, the output parallel code of which is compared by the BS comparison unit with the $N_{max}/2$ code (with a binary basis of the characteristic code).

In converter circuits with automatic characteristic code detection using the bit-by-bit balancing method, the developed order code determination circuit (Fig. 3) is used, consisting of a digital-to-analog code-to-voltage converter (DAC), a reverse register REG_m, a characteristic register REG_v, a comparator *K* and control unit *CU*.

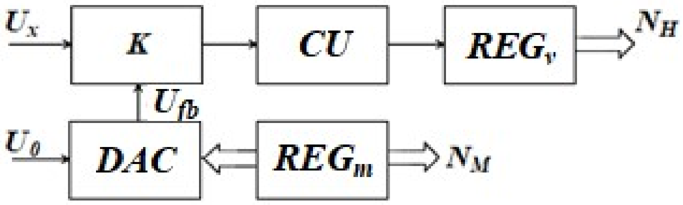

Fig. 3 - Scheme of ADC bitwise balancing with automatic

specification code

In the above scheme, three digits of the N_H characteristic code are determined by shifting the pre-recorded unit in the REG_m register to the right or left by 2^{2-i} digits, where *i* - is the number of the balancing step.

In this case, the feedback voltage generated by the DAC is equal to

$$U_{oc} = U_0 2^{4k_2} 2^{2k_1} 2^{k_0} = U_0 2^{n_h},$$

where U_0 - is the reference voltage applied to the DAC;

k_2, k_1, k_0 - digits of the N_V characteristic code.

III. Conclusion

In this kind of converter circuits, one DAC can be used, some of the bits of which are used in the circuit for determining the characteristic code, and the other part - in the circuit for determining the mantissa code.

It is advisable to use the described ADC circuits for significant ranges of the converted signal, as well as in cases where the a priori the signal level distribution law is close to a logarithmically uniform law, since the quantization characteristic of such converters is close to optimal.

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