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Delay Reducing Design for 2- bit Reversible Comparator Unit

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ABSTRACT: On earth, communication between any organisms is in the form of an analog signal. The manipulation of an analog signal is tedious; therefore analog to digital converter is used to convert the analog signal into digital form. Comparator plays a major role in the signal analysis. In addition to that, comparator circuit provides the efficient and high quality signal, among, the various input signals fed as an input. Magnitude comparator is a technique used to compare, the relation between given inputs in digital form that is in the form of 1's and 0's. Comparison between one or more input signals can be generated by using the relational operators. A comparison using conventional method is less immune to the noise; is a well-known aspect. Taking into an account, the reversible logic gates, which has zero loss of information is used to perform the comparison of two bit input data. In this paper, a comparison is made between the two bit input data. The relative results such as A>B, A<B, A=B are provided for any 2 bit input combinations. The proposed reversible 2-bit comparator module effectively reduces the number of gates used, garbage values and the delay. The delay for reversible 2 bit comparator unit is 6.320 ns. The proposed architecture for the 2-bit reversible comparator using various reversible gates is provided with the output simulated using "ModelSim" and the synthesis report is generated using "Xilinx".

KEYWORDS: Comparator, Reversible logic, Reversible logic gate - M gate, Toffoli gate, MTG gate.

1. INTRODUCTION

In order to process any analog signal, convert the analog signal to digital signal. Analog to Digital convertor aids this conversion. The relation between any digital signals can be made by using the magnitude comparator. Comparator has its own major role in various fields such as railway communication to avoid rail crash, feedback circuitry to compare particular voltage signal in the field of communication, successive approximation techniques. The demerits of the conventional method can be eradicated on using the reversible logic gates. Reversible logic gates have the property of providing zero loss of information while performing any operation over digital signal. The major constraints of reversible logic gates are preventing fan-out and feedback. Taking into consideration, the benefits of using the reversible logic gates; the comparison of 2-bit digital input data is performed using the reversible logic gates. Various reversible logic gates used for implementing the 2-bit reversible comparator are Toffoli gate, M gate and MTG gate. The relative output of the A>B, A<B, A=B is generated using the proposed architecture as shown in fig 4.

1.1. Reversible Logic

The reversible gates endow with one to one mapping between the input and output vectors; do not lose any information. The input and output are uniquely retrievable from each other. The reconstruction of the input data is made possible from the output and the garbage vectors at output state. The reversible logic gate effectively reduces the heat dissipation and hence the loss of information is nullified and thereby allows higher densities and high speed in the manipulation of an arithmetic operation. These gates reduce the complexity of implementation and works in a single clock pulse. The reversible logic Gates have zero fan-out and hence the power dissipation is also zero [1]. The reversible logic gates have garbage values along with the output terms. The number of inputs is equal to the sum of the number of outputs and the number of garbages.

2. REVERSIBLE LOGIC GATE

The reversible logic gates used to implement the 2 bit comparator are Toffoli gate, M gate and MTG gate. The brief description about the reversible logic gates with their logic symbol are as follows:

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2.1 TOFFOLI GATE

Toffoli gates have the property of 3*3 mapping with their input and output vectors [2]. The quantum cost of the Toffoli gate is 5

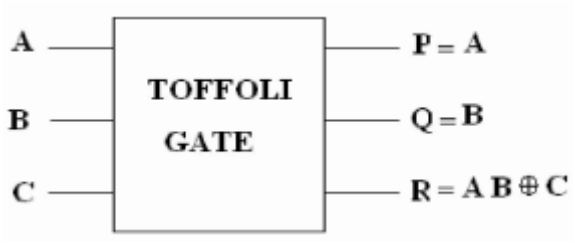

Fig. 1. Reversible logic Toffoli gate.

2.2 M GATE

M gate is a 3*3 gate with 3 input and 3 output vectors [3]. The quantum cost is about 5.

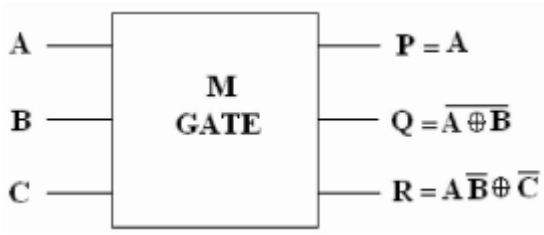

Fig. 2. Reversible logic M gate.

2.3 MTG GATE

MTG gate is a 3*3 input-output mapping gate [4].

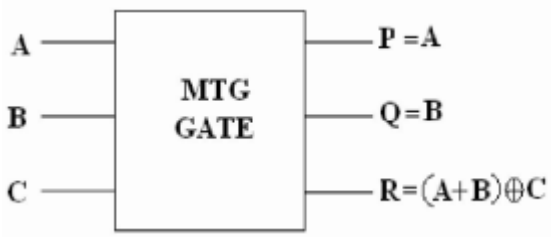

Fig. 3. Reversible logic MTG gate.

3. COMPARATOR

Comparators are dedicated to performing the comparison of two voltages or signals. They provide high signal for A>B, A<B, A=B correspondingly at their respective output ports. Comparator produces the voltage 0 or 1 with respect to the input signal value is above the threshold voltage or below the threshold voltage. Comparator has a wide range of applications such as a null detector to detect the zero signal value, zero crossing detector, relaxation oscillator, level shifter, Analog to digital Convertor, sorting network.

In this paper, the reversible logic gates like M gate, MTG gate and Toffoli gate are used to compare the 2-bit input data. The architecture used for implementing the reversible 2-bit comparator is shown in the fig.4. In this reversible logic implementation, four M gates, three Toffoli gate, two MTG gate were used.

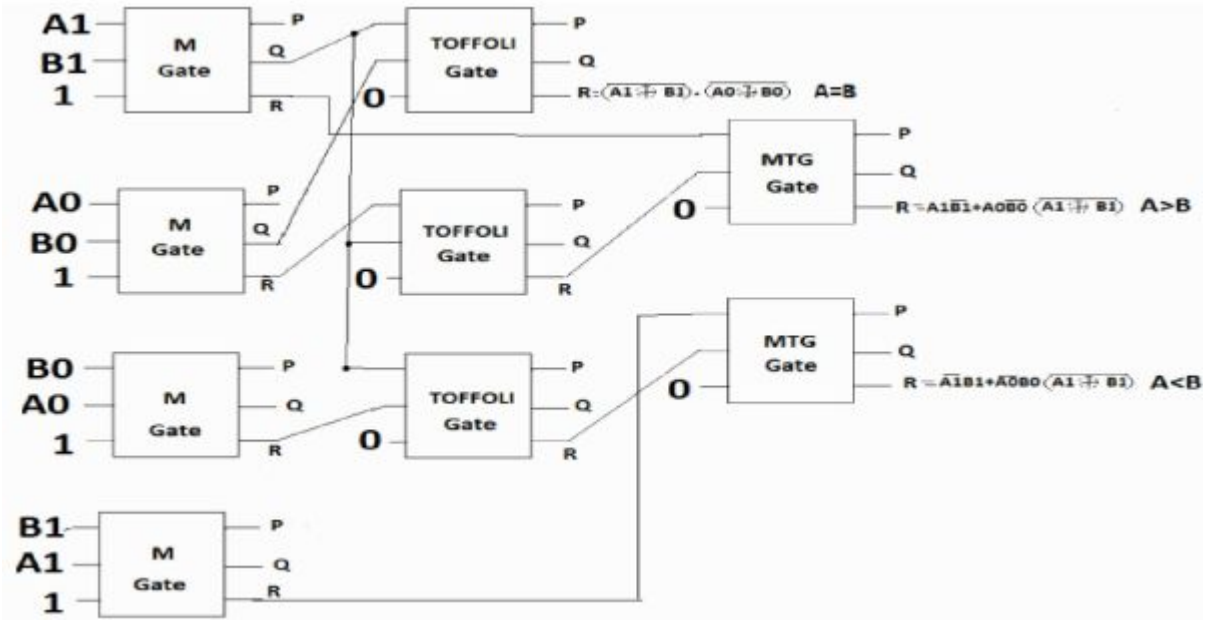

Fig. 4. Architecture of Reversible 2 bit Comparator unit.

This architecture effectively reduces the number of uses of the reversible logic gates. These nine reversible logic gates from fig. 4 were sufficient to implement the reversible 2 bit comparator unit. Four - M gate, 3 Toffoli gate and two MTG gates were used for this purpose of 2 bit reversible magnitude Comparator.

The input for this architecture is in the digital form such as 1's and 0's. So produced output after manipulation is either 1 or 0 on the corresponding output port. '1' specifies the true and the '0' specifies the false value.

CONDITION 1:

The value of A=B, the high value that is '1' is produced at the port corresponding to the A equal to the B relational port and the other port will provide the output as low signal that is '0'. This indicates that the value of A and B are equal in magnitude. The logic expression is shown in the section 3.1.

CONDITION 2:

The value of A<B, the high value that is '1' is produced at the port corresponding to the A less than B relational port and the other port will provide the output as low signal that is '0'. This indicates that the value of A is less than B comparatively, in magnitude. The logic expression is shown in the section 3.2.

CONDITION 3:

The value of A>B, the high value that is '1' is produced at the port corresponding to the A greater than the B relational port and the other port will provide the output as low signal that is '0'. This indicates that the value of A is greater than B comparatively, in magnitude. The logic expression is shown in the section 3.3.

3.1 A = B

In order to perform the relation between A equivalent to B, two M gate and one Toffoli gate are needed. The logic expression to perform A=B is given by [5]:

$$(A1 \oplus B1).(A0 \oplus B0)$$

3.2 A>B

In order to perform the relation between A greater than B, two M gate, one Toffoli gate, one MTG gate are needed. The logic expression to perform A>B is given by [5]:

$$A1\overline{B1}+A0\overline{B0}\,(A1 \oplus B1)$$

3.3 A<B

In order to perform the relation between A less than B, two M gate, one Toffoli gate, one MTG gate are needed. The logic expression used to perform A<B is [5]:

$$\overline{A1}B1+\overline{A0}B0\,(A1 \oplus B1)$$

4. RESULT AND DISCUSSION

The result for the 2- bit comparator is simulated using the simulator called 'ModelSim' is shown in the fig.5.

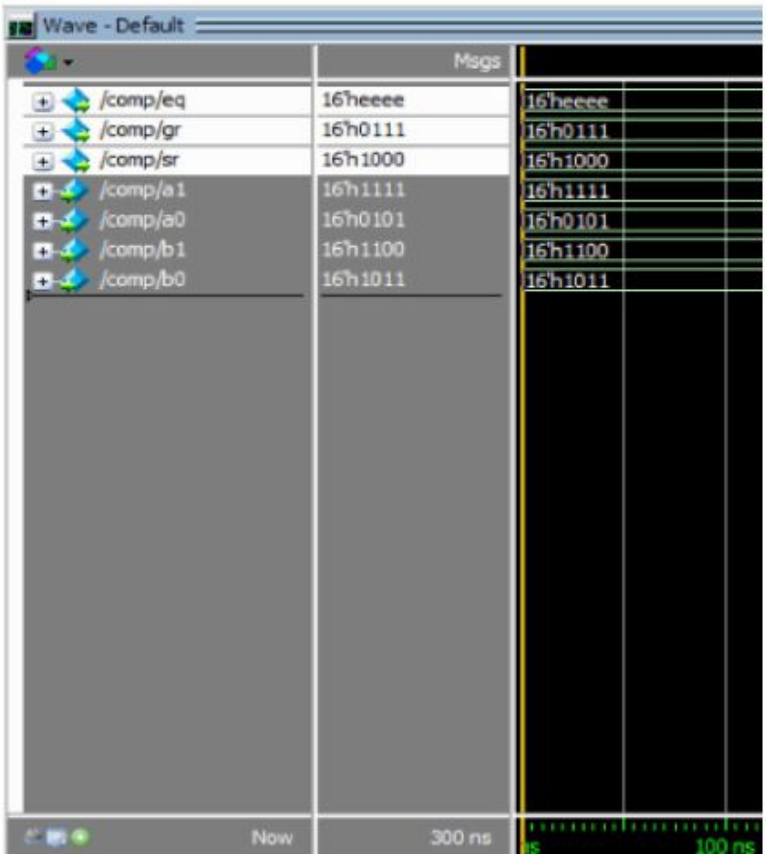

Fig. 5. Simulation Result for Reversible 2-bit Comparator.

From the above result a1,a0,b1,b0 are the inputs where A is compared with B and the relative output for the input fed is produced as the high signal that is '1'; this is produced in the case of the corresponding conditions become true. From the fig

5 port name eq is to display the comparative output if the 2 bit input data is equal. The port name sr provides the result if the value of A is smaller than B. The port gr gives the comparative result of if the value of A is greater than B.

The proposed architecture is implemented over the Spartan 3E kit in the Xilinx synthesizer to know the utilization factors and delay for comparing the 2 bit input data is shown in the table below.

Table 1. Simulation result for 2 bit reversible Comparator unit

Logic Utilization	Used	Available	Utilization
Number of slices	28	960	2%
Number of 4 input LUT	48	1920	2%
Number of bonded IOB's	112	66	169%

The delay calculated for performing the comparison of 2- bit input data is 6.320 ns, which is obtained from 'Xilinx' Synthesizer.

Table 2. Count for number of gates and gabage values for the reversible 2 bit comparator

Name of the gate	Toffoli gate	M gate	MTG gate
Number of gates used	16	32	24
Number of garbage output	48	48	32

From the architecture proposed in this paper, the reversible 2- bit comparator unit requires, the total number of reversible logic gates is 72 which includes sixteen - Toffoli gates, thirty two - M gate, twenty four – MTG gate. The garbage value used for the reversible 2 bit comparator unit is about hundred and twenty four.

5. CONCLUSION

The proposed reversible 2-bit comparator is very efficient when compared to the comparator performed using the transmission gates. On using the transmission gates the delay of processing the comparison operation is 1.038 ms [4]. On the other hand, the proposed reversible architecture can perform the same task of 2 bit comparison at about 6.320 ns. The reversible logic implementation, provide the zero loss of information, hence it can be used widely for all the applications where the comparator plays a role. The proposed logic promises to reduce, the delay for comparing the 2 bit digital input data with reduced number of reversible logic gates and reduced garbage values than the conventional method of comparison.

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